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A Single-Stage High-Frequency Isolated Secondary-Side Controlled AC-DC Converter

Yimian Du[1] and Ashoka K.S. Bhat[1*]
[1] University of Victoria/Department of Electrical and Computer Engineering, Victoria, B.C., Canada
Email: duyimian@ece.uvic.ca, bhat@ece.uvic.ca

***Abstract*—This paper presents a new single-stage high-frequency isolated ac-dc converter that uses a simple control circuit. It is well suitable for wide input variation power sources. The circuit configuration combines a diode rectifier, boost converter and half-bridge dc-dc resonant converter. A high power factor is achieved by discontinuous current mode (DCM) operation of the front-end integrated power factor correction circuit. The output voltage is regulated by fixed-frequency, secondary-side phase-shift active rectifier. Soft-switching operation is achieved for all the switches. This converter operates in three modes, which is classified according to conduction of different switches and diodes. The intervals of operation and steady-state analysis are presented in detail. Design example of a 100 W proposed converter is given together with its simulation and experiment results for wide variation in input voltage.**

***Index Terms*—single-stage, ac-dc converter, DCM, active rectifier, high-frequency isolation, soft-switching**

I. Introduction

Single-phase high-frequency (HF) transformer isolated ac-to-dc converters used in many applications [1-7] ask for following performances: wide variable input range, high power factor and low distortion in ac line current; compact size, simple control strategy and high efficiency. One such application is Permanent Magnet Synchronous Generator (PMSG) based small Wind Energy Conversion System (WECS). The well known conventional approach uses three stages of power conversion: front-end two-stage circuit consisting of a rectifier and a boost converter for power factor correction (PFC) followed by a HF transformer isolated half/ full-bridge dc-to-dc converter as the third stage. This type of approach uses many components resulting in larger size with higher cost and low efficiency. Two approaches are available to reduce the number of stages from three to two and to get improved efficiency: (a) Front-end diode rectifier followed by an integrated dc-dc converter that handles both PFC and HF isolation [1-2]. (b) Introduce active rectifier that achieves PFC instead of uncontrolled diode rectifier followed by HF isolated dc-dc converter [2-5].

Efforts to achieve all the expected functions in a single-stage are reported in [6-7]. In [6], the diode rectifier is integrated with a HF isolated half-bridge resonant converter to form a dual-switch circuit. In [7] two buck-boost dc-dc converters are integrated with two diode rectifiers at the front-end for PFC function and they share switches with a full-bridge series resonant HF isolated dc-dc converter. A high power factor is achieved in [6-7] by operating the input line side in discontinuous current mode (DCM) [8] and the output voltage regulation is achieved by a wide variation in switching frequency. These configurations require a wide variation (almost 2:1) in switching frequency for power control. The dc bus voltage also increases significantly with the increased switching frequency.

Wide variation in switching frequency for power control makes filter design difficult while introducing higher losses at increased frequencies. A higher dc bus voltage results in the requirement of higher voltage devices increasing the conduction losses. To avoid these problems, a single-stage ac-dc converter is proposed in this paper that uses a fixed frequency phase-shift control technique for output voltage regulation.

The concept of secondary-side phase-shift active rectifier used in dc-dc converters [9] is utilized in realizing a fixed-frequency single-stage ac-dc converter. Also, a resonant converter is used in the proposed circuit for guaranteed soft-switching operation.

II. Proposed converter and its operation

The proposed single-phase active rectifier is shown in Fig. 1. At the input side, the diode rectifier is integrated with boost and half-bridge converters to form an integrated rectifier-boost-half-bridge converter (D_{r1}, D_{r2}, S_1, S_2, L_1). The PFC can be achieved by DCM operation of the dual-switch boost converter. A low-pass filter (L_f and C_f) is used for removing HF current harmonics at the ac input line.

A large filter capacitor (C_{bus}) is used to obtain a constant dc bus voltage (V_{bus}). Switches (S_1, S_2) in PFC circuit are shared with a half-bridge resonant converter, which includes two capacitors (C_1, C_2) and a resonant tank circuit (L_r, C_r) placed on the primary-side of HF transformer T_1. A HF active rectifier on the secondary side of T_1 is realized by switches S_3, S_4 and diodes D_{r3}, D_{r4}. The operation of the converter is presented next.

Fixed-frequency complementary gating signals (v_{gs1}, v_{gs2}) and (v_{gs3}, v_{gs4}) of 50% duty cycle and with a small dead-time between them are applied to S_1 and S_2 on the primary-side and to S_3 and S_4 on the secondary-side (Fig. 2). D_{r1}, D_1, S_1 and D_2 handle the positive half-cycle of input voltage. D_{r2}, D_2, S_2 and D_1 serve for the negative half-cycle of input voltage. A high power factor can be achieved by DCM operation in L_1 over the entire line frequency cycle. Both switches operate in zero-voltage switching (ZVS) mode eliminating the turn

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-on switching losses because of the resonant tank circuit. The output voltage can be regulated by the phase-shift between two legs of switches (S_1/S_2 and S_3/S_4).

Based on the relationship between phase-shift angle θ and lagging angle β between v_{ab} and i_r, the proposed converter operates in three modes. Only positive half-cycle of input waveform is considered due to the symmetrical structure. To simplify the operation and analysis, following assumptions are made: (a) All semiconductors and passive components are ideal. (b) Leakage inductance of HF transformer is part of resonant inductor L_r and the effect of magnetizing inductance is neglected. (c) Effects of small dead-gaps between two groups of complementary signals are neglected. Capacitors C_{bus}, C_1, C_2 and C_o are assumed to be large enough so that the dc bus voltage V_{bus} and output voltage V_o can be regarded as constant values.

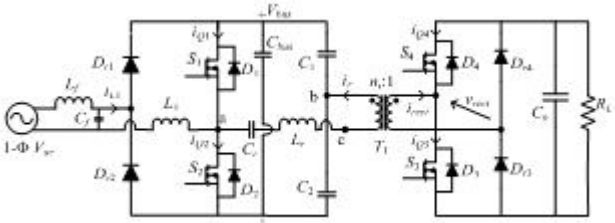

Figure 1. Proposed high-frequency transformer isolated single-phase ac-dc converter

A. Mode 1, $\theta < \beta$

When θ < β, S_1 and S_2 turn-on with ZVS, whereas, S_3 and S_4 turn-off with zero-current-switching (ZCS). The secondary-side HF active rectifier input voltage v_{rect} is a quasi-square waveform because a free-wheeling current flows through the secondary-side of T_1. To understand the operation details of mode 1, the steady-state operation waveforms with a certain value of θ are given in Fig. 2. There are 8 operating intervals in one HF switching period. Devices conducting during different intervals are also marked in Fig. 2. Equivalent circuit for each interval of operation is shown in Fig. 3.

Interval 1 (t_0-t_1): This interval (Fig. 3a) starts when gating signal v_{gs1} is applied at $t = t_0$, gating signal v_{gs4} remains on (v_{gs2} and v_{gs3} are off). During this interval, the current flows through D_{r1} from the ac source. The voltage between a and b (v_{ab}) is positive and is equal to $V_{bus}/2$. The current i_{L1} through boost inductor L_1 starts to increase linearly from zero. D_1 conducts because the resonant current i_r is negative during the interval. Since i_{rect} and i_r are 180° out of phase, D_4 and D_{r3} are conducting on the secondary-side of T_1, hence the HF controlled rectifier input voltage ($v_{rect} = V_o$) is positive and the power is delivered to the load. This interval ends when v_{gs4} is removed (S_4 turns off) and v_{gs3} is given at t_1.

Interval 2 (t_1-t_2): The devices conducting on the primary-side of T_1 is the same as previous interval. Since v_{gs3} is applied, S_3 turns-on and the current flows through S_3 and D_{r3} that result in a free-wheeling loop on the secondary-side of T_1 (Fig. 3b). v_{rect} becomes zero and no power is delivered to the load. This interval ends when i_r reduces to zero at t_2 and S_3 as well as D_{r3} turns-off with ZCS. Boost inductor current i_{L1} continues to increase linearly.

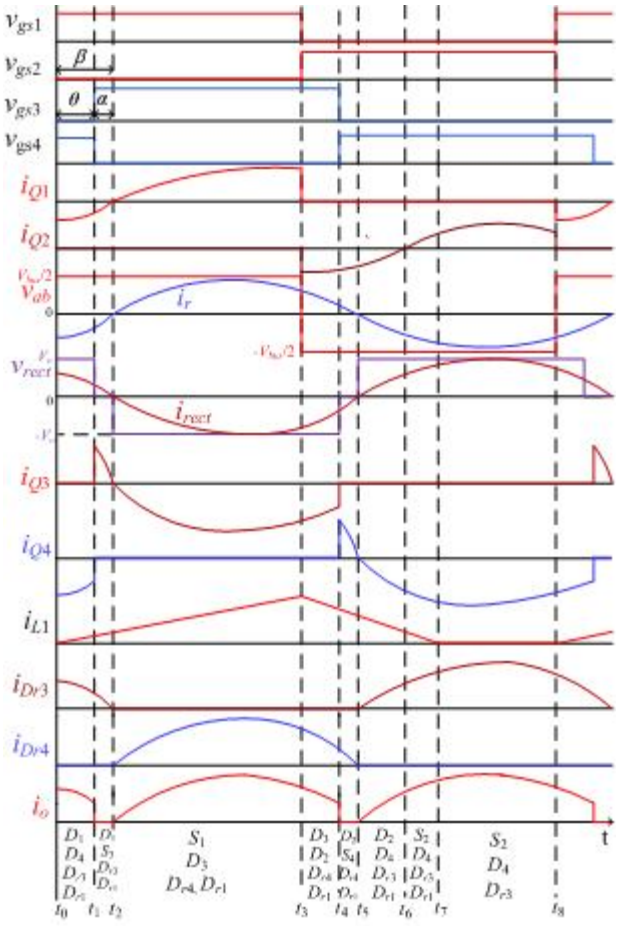

Figure 2. Steady-state waveforms of the proposed converter in one HF cycle for Mode 1 (θ < β).

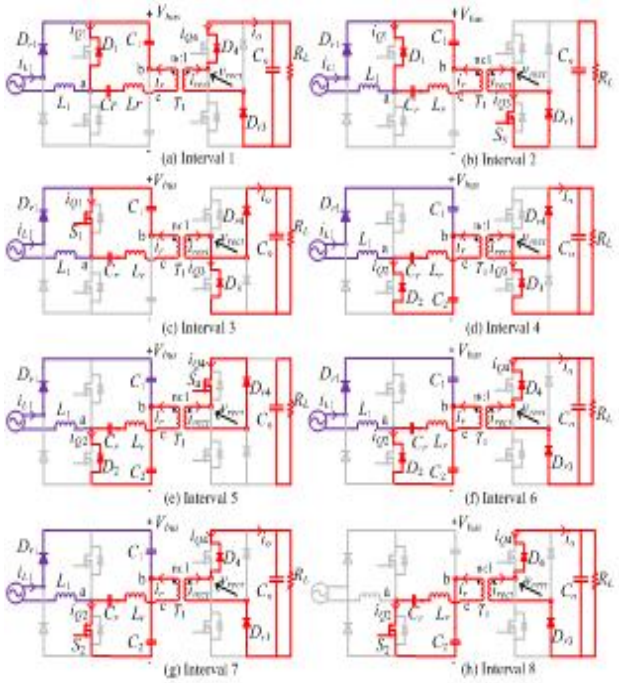

Figure 3. Steady-state equivalent circuits of the proposed converter in one HF cycle for Mode 1.

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Interval 3 (t_2-t_3): When i_r becomes positive, S_1 turns on with ZVS mode. On the secondary-side, D_3 turns-on allowing the current to flow through D_3 and D_{r4} and power is delivered to the load (Fig. 3c). Current i_{L1} continues to increase linearly in this interval and reaches its peak value when v_{gs1} to S_1 is removed at t_3. Half of one HF switching cycle has ended at the end of this interval.

Interval 4 (t_3-t_4): This interval starts when v_{gs1} is removed and v_{gs2} is applied. v_{ab} changes its polarity from positive to negative, $v_{ab} = -V_{bus}/2$. On primary-side of T_1, since S_1 is turned-off D_2 begins to conduct (Fig. 3d), and i_{L1} decreases linearly from its peak value. Power continues to be delivered to the load through D_3 and D_{r4}. The interval ends when gating signal v_{gs3} is removed.

Interval 5 (t_4-t_5): Since v_{gs3} is removed and v_{gs4} is applied at the beginning of this interval, S_4 turns-on and the current flows through S_4 and D_{r4} that result in a free-wheeling loop on the secondary-side of T_1 (Fig. 3e). v_{rect} becomes zero and no power is delivered to the load. The devices conducting on the primary-side of T_1 are the same as previous interval. This interval ends when i_r goes to zero at t_5, S_4 and D_{r4} turns-off with ZCS and i_{L1} continues to decrease linearly.

Interval 6 (t_5-t_6): In this interval, the polarity of i_r has changed from positive to negative. On the secondary-side of T_1, D_4 and D_{r3} turn-on with ZCS and power is supplied to the load (Fig. 3f). At $t = t_6$, i_{Q2} (i.e. current through D_2) reaches zero and current i_{L1} continues to decrease linearly.

Interval 7 (t_6-t_7): At $t = t_6$, S_2 turns on with ZVS mode. The other devices conducting remain the same as Interval 6 (Fig. 3g). At the end of this interval, $t = t_7$, i_{L1} decreases to zero and D_{r1} turns-off with ZCS.

Interval 8 (t_7-t_8): Since D_{r1} and D_{r2} are not conducting, $i_{L1} = 0$. S_2 is conducting and energy stored in the circuit is still delivered to the load through D_4 and D_{r3} (Fig. 3h). At $t = t_8$, one HF switching cycle has completed and next cycle begins.

B. Mode 2, $\theta = \beta$

In this mode, S_1 and S_2 operate with ZVS turn-ON. The HF active rectifier works as a typical diode rectifier. Current flows only through D_3 and D_4, switches S_3 and S_4 do not conduct even though v_{gs3} and v_{gs4} are applied. The secondary-side HF active rectifier input voltage (v_{rect}) is a square waveform since there is no free-wheeling interval. Therefore, energy is delivered to the load continuously. All currents and voltages on the secondary side of T_1 are the same as those when a diode rectifier is used on the secondary-side of T_1. The details of the Mode 2 will not be presented here.

C. Mode 3, $\theta > \beta$

If θ is larger than β, all the switches, S_1 - S_4, operate with ZVS turn-ON. On the secondary-side, HF active rectifier input voltage v_{rect} is a quasi-square waveform because a freewheeling current flows through the secondary-side of T_1. In this mode, there are 7 operating intervals in one HF switching period as shown in the steady-state waveforms of Fig. 4. Devices conducting during different intervals are also marked in Fig. 4 and equivalent circuits for operation are shown in Fig. 5.

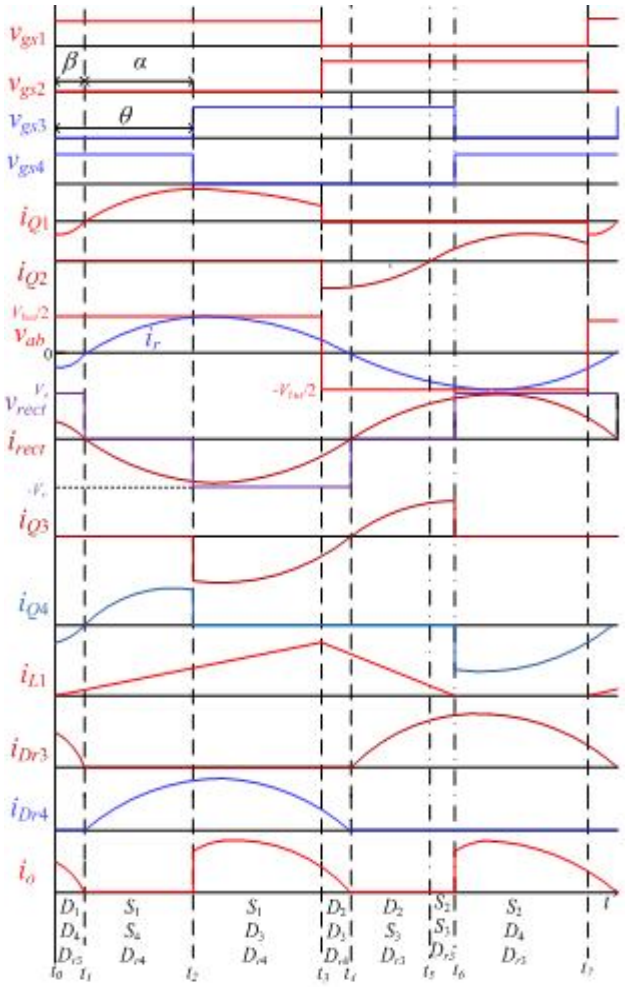

Figure 4. Steady-state waveforms of the proposed converter in one HF cycle for Mode 3 (θ > β). Note: D_{r1} is conducting for intervals 1 to 6.

Interval 1 (t_0-t_1): Operation of this interval (Fig. 5a) is same as interval-1 of Mode 1. This interval ends when i_r and i_{rect} reach zero at t_2, hence i_{Q1} and i_{Q4} also reach zero turning off Q_1 and Q_4 with ZCS. Also, D_{r3} turns-off with ZCS and D_{r4} turns-on with ZCS.

Interval 2 (t_1-t_2): In this interval (Fig. 5b), since gating signals have been already given to S_1 and S_4 both turn on with ZVS mode. On the secondary-side of T_1, free-wheeling current flows through D_{r4} and S_4, resulting in zero voltage across the secondary winding, $v_{rect} = 0$. This interval ends when the gating signal v_{gs4} is removed and v_{gs3} is given to S_3 at t_2, current i_{L1} continues to increase linearly.

Interval 3 (t_2-t_3): Since v_{gs4} is removed and v_{gs3} was given to S_3 at the end of last interval, S_4 turns-off and D_3 starts conducting together with D_{r4} (Fig. 5c) delivering power to the load. Gating signal v_{gs1} to S_1 is removed at t_3. Boost inductor current i_{L1} continues to increase linearly in this interval and reaches its peak value at t_3.

Interval 4 (t_3-t_4): Since v_{gs1} was removed and v_{gs2} was given to S_2 at t_3, the polarity of v_{ab} changes from positive to negative, $v_{ab} = -V_{bus}/2$. D_2 starts to conduct and i_{L1} begins to decrease side of T_1 remains the same as interval 3 (Fig. 5d). Power is still delivered to the load.

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This interval ends when i_r and i_{rect} reach zero at t_4, hence i_{Q3} and i_{DR4} also reach zero, i.e., D_3, D_{r4} turn off with ZCS.

Interval 5 (t_4-t_5): The devices conducting on the primary-side of T_1 are the same as previous interval. S_3 turns on with ZVS mode and the current flows through S_3 and D_{r3} that result in a free-wheeling loop on the secondary-side of T_1 (Fig. 5e). v_{rect} becomes zero and no power is delivered to the load. Current i_{L1} continues to decrease linearly and i_{Q2} becomes zero (D_2 turns off with ZCS) at the end of this interval.

Interval 6 (t_5-t_6): Since gating signal is already given to S_2, S_2 is turned on with ZVS mode since current through its anti-parallel diode reached zero at the end of last interval. On the secondary-side, devices conducting are the same as last interval with v_{rect} = 0 and no output power is delivered (Fig. 5f). At $t = t_6$, i_{L1} decreases to zero and D_{r1} turns-off with ZCS.

Interval 7 (t_6-t_7): This interval (Fig. 5g) is the same as the interval-8 of Mode 1. At $t = t_7$, one HF switching cycle has completed and it is ready for next cycle.

The intervals shown above are for certain values of phase-shift for three typical modes. If different values of phase-shift are given, sequence of intervals might be different, but the soft-switching operation in these modes is guaranteed.

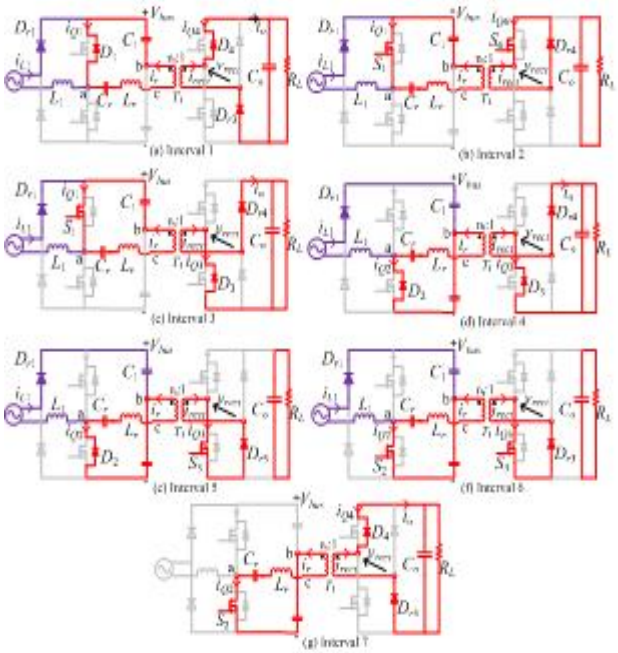

Figure 5. Steady-state equivalent circuits of the proposed converter in one HF cycle for Mode 3.

III. Steady-State Analysis

For analysis purpose, the single-stage converter can be viewed as two separate parts: (i) front-end PFC circuit and (ii) half-bridge resonant converter with secondary-side HF active rectifier. The PFC circuit operates in DCM mode and its analysis is well known [2,8].

The steady-state analysis of the half-bridge resonant converter with secondary-side HF active rectifier is done using approximate analysis (i.e., using fundamental components in the Fourier series of waveforms, neglecting higher harmonics) approach [10,11] and is presented next.

All parameters on the secondary-side of the HF transformer are reflected to primary side of T_1, which are denoted by the superscript "' ". To get generalized design curves, all the parameters are normalized using the base values: $V_B = V_{bus,max}/2$, $Z_B = R'_L$, $I_B = V_B/Z_B$. The Half-bridge converter gain is defined as $M = V_O'/(0.5V_{bus})$. The normalized switching frequency is given by $F = \omega_s/\omega_r = f_s/f_r$ where resonant frequency $\omega_r = 2\pi f_r = 1/(\sqrt{L_r C_r})$ and switching frequency, $f_s = \omega_s/(2\pi)$. The normalized values of all reactances are given by $X_{Lr,pu} = QF$, $X_{Cr,pu} = -Q/F$, $X_{s,pu} = X_{Lr,pu} + X_{Cr,pu} = Q(F - 1/F)$, where $Q = \omega_r L_r/R'_L$.

Since it is preferred that all switches operate in ZVS mode, the proposed converter should preferably operate in Mode 2 and Mode 3. Therefore, the following analysis presented is based on the preferred modes 2 and 3.

In the approximate analysis first step is to replace the HF active rectifier by ac equivalent impedance (Z_{ac}). Fig. 6 shows the HF active rectifier diagram with all voltages and currents referred to primary-side of T_1. Assume V'_O is constant due to the large filter capacitor across the load. β is the lagging angle between V_{ab} and i_r, and θ is the controlled phase-shift angle. The HF active rectifier input voltage V'_{rect} is a quasi-square wave with an amplitude of $\pm V'_o$ and pulse width of (π+β–θ). Resonant current i_r lags the voltage v_{ab} by β and fundamental component of V'_{rect} lags v_{ab} by $[\beta + \frac{\theta-\beta}{2}] = (\theta+\beta)/2$. Define α = (θ – β), (π+β–θ) = (π – α).

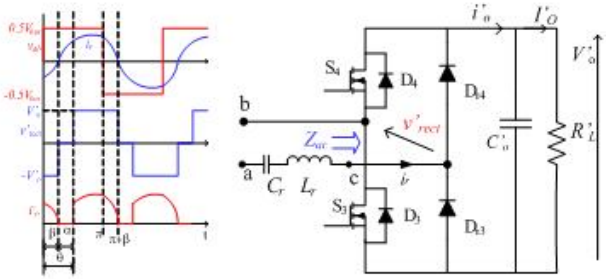

Figure 6. Voltages and currents in HF active rectifier, all parameters referred to primary-side.

The equations for the instantaneous values of fundamental components of the voltage (v_{ab}) across the output terminals *a* and *b*; resonant current i_r; and rectifier input voltage (v'_{rect}) referred to primary-side are given by

$$v_{ab1} = \sqrt{2}V_{ab1}\sin(\omega_s t) = \sqrt{2}\frac{4(V_{bus}/2)}{\sqrt{2}\pi}\sin(\omega_s t) \text{ V}, \quad (1)$$

$$i_r = \sqrt{2}I_r \sin(\omega_s t - \beta) \text{ A}, \quad (2)$$

$$v'_{rect1} = \sqrt{2}V'_{rect1}\sin(\omega_s t - (\beta + \frac{\alpha}{2})) \text{ V}, \quad (3)$$

where V_{ab1} = rms value of fundamental component of v_{ab}, I_r = rms value of the resonant current, and V'_{rect1} = rms value of the fundamental component of v'_{rect} given by

$$V'_{rect1} = \frac{4V'_o}{\sqrt{2}\pi}\sin\left(\frac{\pi+\beta-\theta}{2}\right) = \frac{4V'_o}{\sqrt{2}\pi}\cos\left(\frac{\alpha}{2}\right) \text{ V}. \quad (4)$$

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If θ = β, the active rectifier operates in Mode 2, i.e., it acts as a diode rectifier. The load current I'_o is the average value of i'_r, which is obtained as

$$I'_o = \frac{1}{\pi}\int_{\theta}^{\pi+\beta} \sqrt{2} I_r \sin(\omega_s t - \beta)\, d\omega_s t = \frac{2\sqrt{2} I_r}{\pi} \cos^2\left(\frac{\alpha}{2}\right) \quad \text{A} \qquad (5)$$

So the rms value of HF rectifier input (same as the resonant) current i_r is given by

$$I_r = \frac{\pi I'_o}{2\sqrt{2}\cos^2\left(\frac{\alpha}{2}\right)} \quad \text{A} \qquad (6)$$

Note that V'_{rect} and i_r are not in phase, so the ac impedance (looking into terminals "bc") can be written as

$$Z_{ac} = \frac{V'_{rect1}\angle -(\beta+\alpha/2)}{I_r \angle -\beta} = |Z_{ac}|\angle \frac{-\alpha}{2} \quad \Omega \qquad (7)$$

Using (4) and (6)

$$|Z_{ac}| = \frac{V'_{rect1}}{I_r} = \frac{8R'_L}{\pi^2}\cos^3\left(\frac{\alpha}{2}\right) \quad \Omega \qquad (8)$$

where primary side referred load resistance, $R'_L = V'_o/I'_o\ \Omega$. The output power (assumed to be same as the rectifier input power since losses are neglected) is given by

$$P_o = V'_{rect1} I_r \cos(\alpha/2) \quad \text{W} \qquad (9)$$

The half-bridge converter voltage gain in the phasor circuit shown in Fig. 7 can be evaluated as follows:

$$\left|\frac{V'_{rect1}}{V_{ab1}}\right| = \frac{|Z_{ac}|}{|Z_{ac}+jX_s|} = \frac{1}{\sqrt{A^2+\left(\frac{\pi^2 Q(F-1/F)}{8A^3}-\sqrt{1-A^2}\right)^2}} \qquad (10)$$

where $X_s = Q(F-1/F)R'_L$, and $A = \cos(\alpha/2)$
Also using (1) and (4),

$$\frac{V'_{rect1}}{V_{ab1}} = \frac{V'_o}{0.5V_{bus}}\cos\left(\frac{\alpha}{2}\right) \qquad (11)$$

Therefore using (10) and (11), the normalized half-bridge voltage gain M (output voltage to bus voltage) is given by the following expression

$$M = \frac{V'_o}{0.5V_{bus}} = \frac{1/A}{\sqrt{A^2+\left(\frac{\pi^2 Q(F-1/F)}{8A^3}-\sqrt{1-A^2}\right)^2}} \qquad (12)$$

Using (1), the normalized tank peak current is

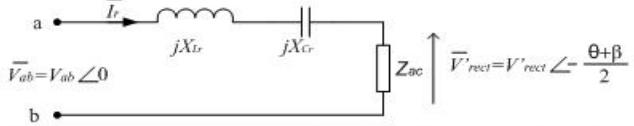

Figure 7. Phasor equivalent circuit of the half-bridge converter used for approximate analysis.

$$I_{rp,pu} = \frac{\sqrt{2}V_{ab1,pu}}{|Z_{ac,pu}+jX_{s,pu}|} = \frac{\pi}{2A^3\sqrt{A^2+\left(\frac{\pi^2 Q(F-1/F)}{8A^3}-\sqrt{1-A^2}\right)^2}} \qquad (13)$$

Then the normalized resonant capacitor peak voltage is

$$V_{crp,pu} = I_{rp,pu}X_{Cr,pu} = I_{rp,pu}(Q/F) \quad \text{p.u.} \qquad (14)$$

The angle β between v_{ab} and i_r is obtained as

$$\tan\beta = \frac{\pi^2 Q\,(F-1/F)}{8A^4} - \frac{\sqrt{1-A^2}}{A} \qquad (15)$$

In this case, V_{bus} decreases with increasing value of θ due to the fixed duty cycle of gating signals applied to S_1/S_2. According to (8), the load of the proposed ac-dc converter $|Z_{ac}|$changes with θ rising. In order to find the relationship between V_{bus} and θ, power balance concept (assuming 100% efficiency) is employed as follows: the ac input real power P_{in} is given by [2, 8].

$$P_{in} = \frac{V_m^2 D^2 y}{2\pi L_1 f_s} \quad \text{W} \qquad (16,a)$$

where V_m is peak value of ac input voltage, D=0.5 is the duty cycle of S_1/S_2, y is a function of V_m/V_{bus}.

The ac-dc converter output is given by

$$P_o = \frac{V_o^2}{R_L} = \frac{(0.5V_{bus}M/n_t)^2}{R_L} \quad \text{W} \qquad (16,b)$$

Assuming an ideal case (100% of efficiency), $P_{in} = P_o$, we obtain

$$\frac{V_m^2 D^2 y}{2\pi L_1 f_s} = \frac{(0.5V_{bus}M/n_t)^2}{R_L}, \quad \text{W} \qquad (17,a)$$

Equation (17a) can be re-arranged as

$$\frac{V_m}{V_{bus}} = M\sqrt{\frac{2\pi L_1 f_s}{4n_t^2 D^2 R_L y}} \quad \text{W} \qquad (17,b)$$

Therefore, using (12) and (17b), the proposed ac-dc converter gain is given by

$$\frac{V'_o}{V_m} = \frac{V'_o/V_{bus}}{V_m/V_{bus}} = \frac{M/2}{V_m/V_{bus}}. \quad \text{W} \qquad (18)$$

Using the equations derived above, various design curves are obtained. Using (12) and (15), normalized half-bridge converter gain M versus phase-shift angle θ for various values of normalized switching frequency F with Q = 0.9 is shown in Fig. 8(a). Similarly, Fig. 8(b) shows the converter gain M versus phase-shift angle θ for various values of Q with normalized switching frequency F = 1.1. Using (12)-(16), the normalized peak tank current $I_{rp,pu}$ and normalized peak capacitor voltage $V_{Crp,pu}$ versus half-bridge converter gain M obtained are shown in Figs. 8(c) to (e), respectively. The tank kVA/kW of output power versus M for different values of Q is plotted in Fig. 8(f).

According to Figs. 8(a) and 8(b), M starts to increase, reaches its peak value and then decreases as the value of θ is increased. Note that for the same value of θ, smaller values of F and Q bring higher value of M. The proposed converter is supposed to operate in the rising part of the design curves to get enough gain since the converter should operate with wide variation (1:2) in input voltage. Figs. 8(c) to 8(e) show that smaller values of F and Q results in lower peak values for the resonant current and the resonant capacitor voltage. In Fig. 8(f), a smaller

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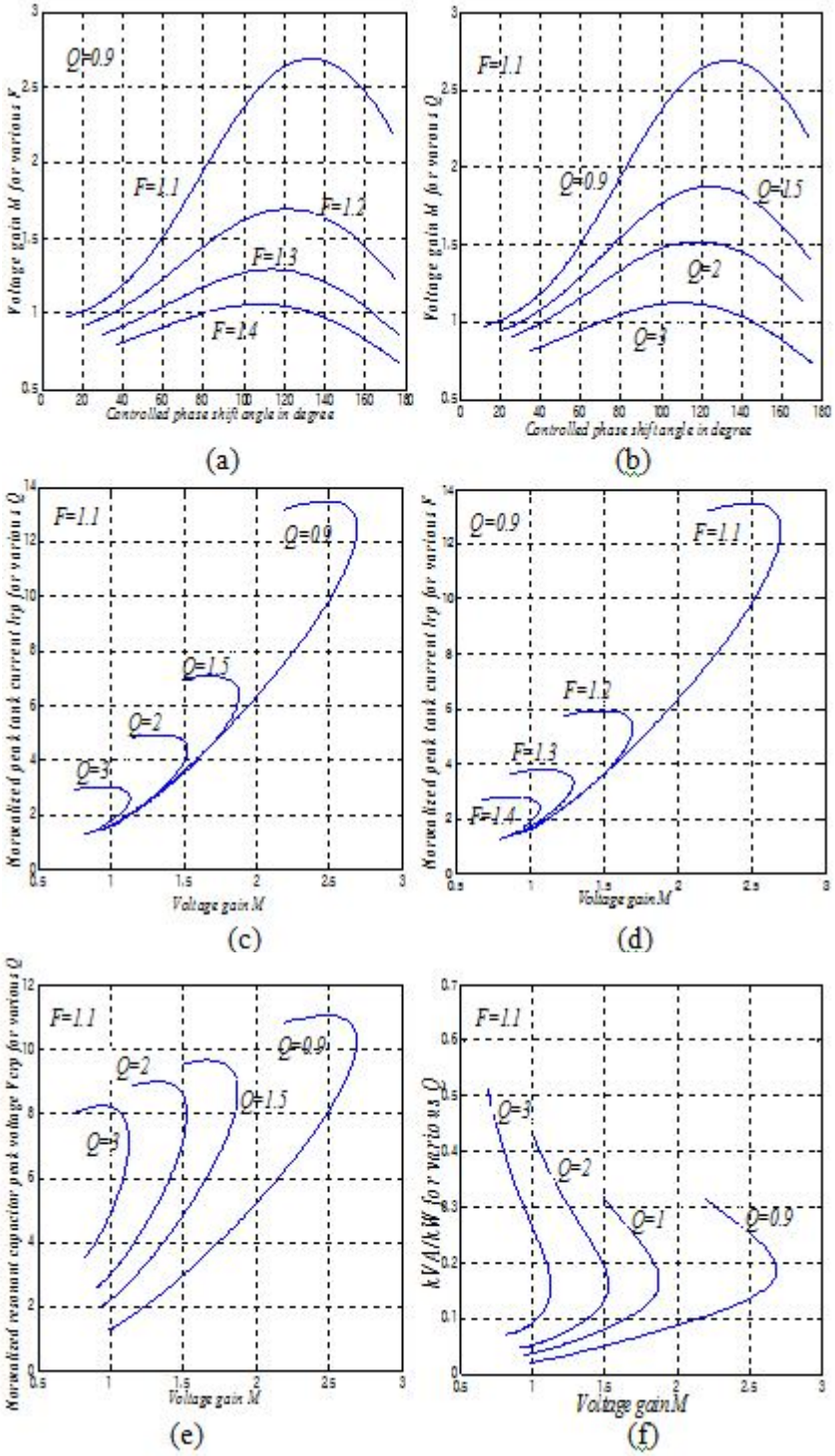

Figure 8. (a) Normalized voltage gain (M) vs phase shift angle (θ) for various values of normalized switching frequency F, (F = 1.1 to 1.4), Q = 0.9; (b) M vs phase shift angle for various values of Q (Q = 0.9 to 3), F =1.1; (c) normalized tank peak current vs M for different values of Q (Q = 0.9 to 3), F=1.1; (d) normalized tank peak current vs M for different values of F (F = 1.1 to 1.4), Q = 0.9; (e) normalized peak capacitor voltage vs M for various values of Q (Q = 0.9 to 3), F=1.1; (f) tank kVA/kW of output power vs M for different values of Q, (Q = 0.9 to 3). value of Q brings smaller value of tank kVA/kW of output power. Based on the above observations, optimum values chosen in the present design are F = 1.1 and Q = 0.9; dc-dc converter gain, M = 0.97.

IV. Design Example, Simulation and experimetal Results

A. Design

A design example with the following specifications is given to illustrate the design procedure: ac input voltage (peak value), V_m = 75-150 V, 60Hz; output voltage, V_o = 100 V; output power, P_o = 100 W; switching frequency, f_s = 100 kHz.

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Using the equations given in [2,8]: $V_B = V_{m,\max} = 0.5V_{bus,\max}$ = 150 V, D = 0.5, f_s = 100 kHz, we calculate L_1 = 248.88 mH.

In designing the converter, the optimum values chosen in Section III will be used, i.e., F = 1.1; Q = 0.9; and dc-dc converter gain, M = 0.97. It is also preferred that when the maximum input voltage is applied, the proposed converter is operating in Mode 2 to ensure the operation of switches in ZVS mode when phase-shift is applied.

Given $I_o = P_o/V_o$ = 1 A, $R_L = V_o/I_o$ = 100 W. Using (15) with θ = β for Mode-2, β = 9.75°. Hence the phase-shift must be adjusted to θ = β = 9.75° when the maximum input voltage is applied under full-load condition to ensure the converter operation in Mode 2. With the phase-shift increased, the converter operates in Mode 3.

On the primary-side of T_1 reflected output voltage, V_o' = MV_B = 145.5 V, and the transformer ratio is n_t :1 = V_o' :V_o =1.455:1. The reflected load resistance value is $R'_L = n_t^2 R_L = 211.7\,\Omega$. Based on (12), (17b) and other specifications in the example, V_m/V_{bus} as a function of θ is plotted as Fig. 9, where M reaches its peak value M = 2.7 (Fig. 8(a) and (b)) at θ = 130° and using (17b) the corresponding value of V_m/V_{bus} = 0.66. Hence the maximum value of the proposed converter gain can be calculated using (18), which gives V_o'/V_m = 2.05. It is suitable for the wide input variation of the design example.

Using $Q = 0.9 = \sqrt{L_r/C_r}/R'_L$ and $F = 1.1 = \omega_s\sqrt{L_rC_r}$, the tank parameters can be calculated as

$$L_r = 331.28\ \mu\text{H and } C_r = 9.252\ \text{nF}.$$

B. PSIM Simulated Results

In order to verify design, the software PSIM 6.0 is used to simulate the design example. A fixed step of 0.1 μs is chosen for the simulation. The simulation results are shown for V_m = 150V (Fig. 9(a), Mode 2) and 75V (Fig. 9(b), Mode 3), respectively. When $V_{m,\max}$ = 150V is applied, θ is set as 6° in order to make sure the proposed converter is operating in Mode 2. In Fig. 9(a), the secondary-side active rectifier works as a diode rectifier due to the current flowing through D_{r3}/D_{r4} as predicted. As expected, v_{rect} is a square wave. We observe a high power factor (0.99) and low total harmonic distortion (THD) (12.5%) for the input line current due to the DCM operation of i_{L1}. V_{bus} is twice of $V_{m,\max}$ because of the 50% duty cycle of front-end dual-switch boost converter operation. Also S_1/S_2 operates in ZVS mode. When the minimum input voltage $V_{m,\min}$ = 75 V is applied in Fig. 9(b), θ is adjusted to 130° in order to obtain enough boost gain for regulating the output voltage. v_{rect} becomes a quasi-square wave due to operating interval 2,5,6 in Mode 3. V_{bus} is less than twice of $V_{m,\min}$ as expected (V_m/V_{bus} = 0.66 in Fig. 10). All switches work in ZVS mode. A lower power factor (0.87) and higher THD (56.2%) for the input line current are obtained since i_{L1} loses DCM operation in parts of line frequency cycle. These waveforms confirm the theory.

Figure 9: Simulation results for (a) V_m = 150 V and (b) V_m = 75 V. Waveforms shown from top to bottom for each case: (i) line voltage, line current, bus voltage, load voltage; (ii) primary-side switch currents i_{Q1} and i_{Q2}, current through L_1 (i_{L1}); (iii) secondary-side switch currents i_{Q3} and i_{Q4}, rectified output current before filtering (i_o); (iv) v_{ab} and resonant current i_r, HF rectifier input voltage (v_{rect}) and current (i_{rect}), resonant capacitor voltage (v_{cr}).

C. Experiment Results

A 100 W laboratory prototype was built based on the design example presented above. The detailed values of MOSFET switches and passive components are listed in Table I. A DSP board (eZdspS320F2812) is used to generate phase-shifted PWM gating signals. The converter is operated in open-loop control for wide input voltage of 150V to 75V (peak). The experimental results are shown for V_m = 150V (Fig. 11(a), Mode 2) and 75V (Fig. 11(b), Mode 3), respectively. Input line voltage and line current waveforms together with HF waveforms are given in Fig. 11. Note that input pf = 0.98, THD = 17% at $V_{m,\max}$ = 150V, θ = 10°, and pf = 0.88, THD = 53.7% at $V_{m,\min}$ = 75V, θ = 133°. Comparing the simulated waveforms with the experimental ones, they are not much different, and these waveforms confirm the theory and simulated results.

Table II summarizes and compares theoretical, simulated and experimental results. Every group of data among theory, simulation and experiment is close enough.

V. Conclusions

A new single-phase, single-stage active ac-dc converter is proposed and studied in this paper. The circuit is a single-stage configuration that integrates diode rectifier, boost chopper and HF isolated resonant dc–dc converter. Hence it includes functions of rectification, natural PFC (without active feedback control) and HF isolation, which is well suitable for several applications including PMSG-based small WECS. The output voltage is regulated by a fixed frequency, secondary-side phase-shift control strategy. All switches operate in soft-switching mode for the entire range of variations in input voltage due to the use of resonant converter and leakage inductance is used as part of resonant inductor.

The proposed converter operates in three modes depending on the conduction of different switches and diodes. The preferred Mode 2 and Mode 3 are analyzed using approximate ac circuit analysis approach. Design curves have been obtained using the analysis and a design example is presented to illustrate the design procedure. Using the values obtained in the design example, PSIM simulation and experiment were done and results obtained have been presented. The experimental results show good agreement with the theoretical analysis and simulated results. One problem with the proposed converter is low PF and higher THD for low line current. This problem will be solved in the future work.

Figure 11: Experiment results for (a) V_m = 150 V and (b) V_m = 75 V. Waveforms shown from top to bottom for each case: (i) line voltage (50V/div for (a), 20V/div for (b), ch4), line current (1A/div, ch3), time scale 2ms/div; (ii) FFT of input line current, 0.25A/div, 68.27Hz/div; (iii) v_{ab} (100V/div, ch1), HF rectifier input voltage v_{rect} (100V/div, ch2), resonant current i_r (1A/div

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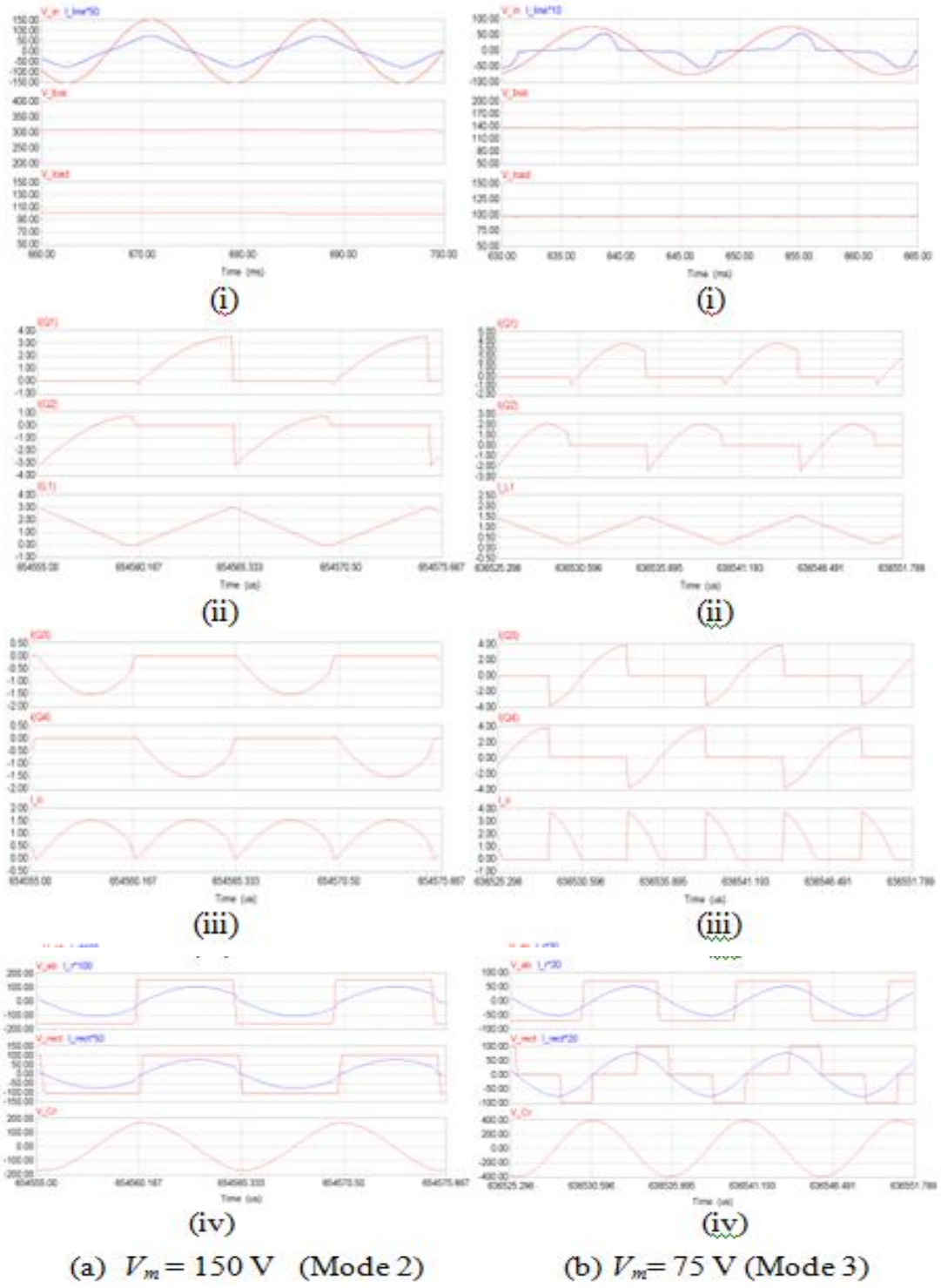
for (a), 2.5A/div for (b) ,ch3); (iv) resonant capacitor voltage v_{cr} (100V/div, ch4); (v) boost inductance current i_{L1} (1A/div, ch3), time scale in (iii)-(v) : 2ms/div.



(a) $V_m = 150$ V (Mode 2) (b) $V_m = 75$ V (Mode 3)

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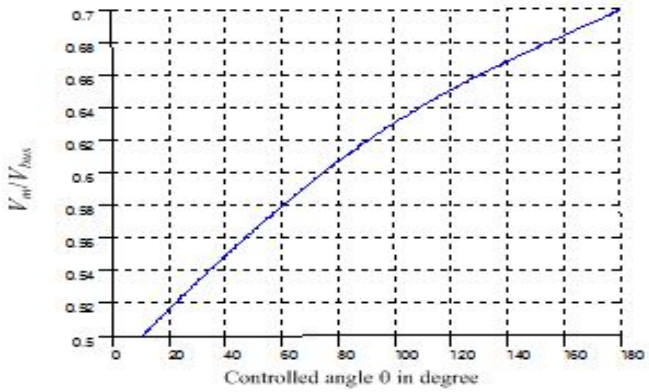
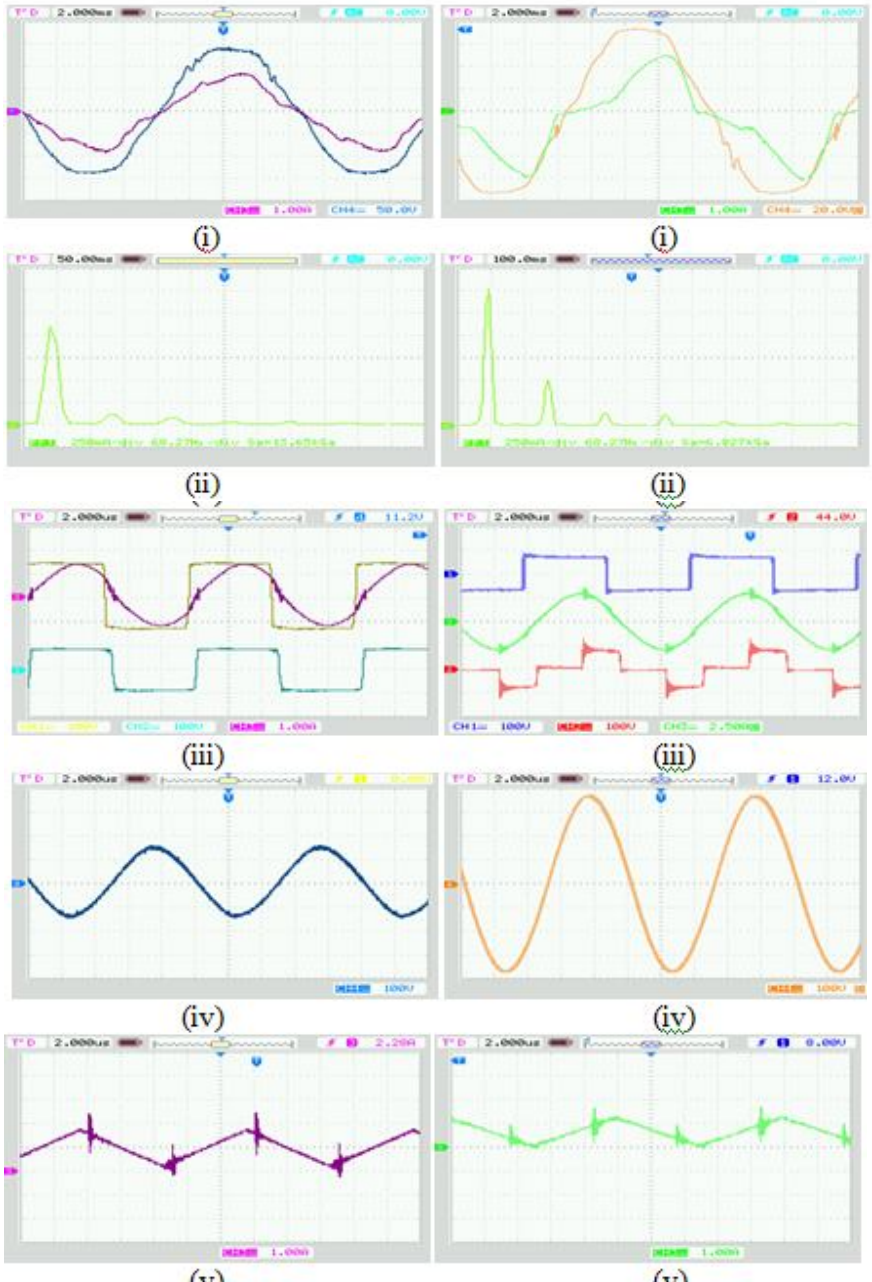


Figure 10. V_m/V_{bus} vs θ (in degree) for the example (using numerical solution of (17b)).



(a) V_m= 150 V (Mode 2) (b) V_m = 75 V (Mode 3)

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TABLE I.
COMPONENTS USED IN EXPERIMENT

S_1/ S_2, S_3/S_4	MOSFETs: G20N50C, G22 N60S
D_1/D_2, D_3/D_4	U1560, RHRP1560
C_{bus}, C_1, C_2, C_o	400 μF
L_1, L_r^{**}, C_r	248 μH, 310 μH*, 10.4nF
L_f, C_f	3 mH, 1 μF
HF transformer	Core: TDK EI60, material 2500B2 Turns ratio: 14 : 10

**Including leakage inductance of HF transformer

TABLE II.
COMPARISON OF THEORETICAL, SIMULATED AND EXPERIMENTAL RESULTS

	$V_{m,max}$ = 150V (Mode 2)			$V_{m,min}$ = 75V (Mode 3)		
	theory	simn	expt	theory	simn	expt
$I_{in,rms}$ (A)	-	0.965	0.98	-	2.49	2.1
pf	-	0.99	0.98	-	0.87	0.88
*$THD(i_{line})$	-	12.5%	17%	-	56.2%	53.7%
V_o (V)	100	100.3	95.2	100	97.3	91.8
V_{bus} (V)	300	305.9	296	113.6	131	114
θ	9.75°	6°	10 °	130°	130°	133°
$I_{r,pk}$ (A)	1.09	1.04	1.2	2.97	2.81	3.38
$V_{cr,pk}$ (V)	134.7	168.6	150	363.7	398.2	368
efficiency	-	-	90%	-	-	86%

*Using harmonic number up to 9

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